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<b>TRANSMITTAL FORM</b>  <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/944,506	
	Filing Date	August 30, 2001	
	First Named Inventor	Pai-Hung Pan	
	Art Unit	2823	
	Examiner Name	G. Fourson III	
Total Number of Pages in This Submission		Attorney Docket Number	2269-2919.5US (96-0499.02/US)

ENCLOSURES (check all that apply)		
<input type="checkbox"/> Fee Transmittal Form  <input type="checkbox"/> Fee Attached  <input type="checkbox"/> Amendment / Reply  <input type="checkbox"/> After Final  <input type="checkbox"/> Affidavits/declaration(s)  <input type="checkbox"/> Extension of Time Request  <input type="checkbox"/> Express Abandonment Request  <input type="checkbox"/> Information Disclosure Statement  <input type="checkbox"/> Certified Copy of Priority Document(s)  <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application  <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s)  <input type="checkbox"/> Licensing-related Papers  <input type="checkbox"/> Petition  <input type="checkbox"/> Petition to Convert to a Provisional Application  <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address  <input type="checkbox"/> Terminal Disclaimer  <input type="checkbox"/> Request for Refund  <input type="checkbox"/> CD, Number of CD(s) _____  <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC  <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences  <input checked="" type="checkbox"/> Appeal Brief (13 pages); Claims Appendix (5 pages)  <input checked="" type="checkbox"/> Communication Accompanying Appeal Brief (2 pages)  <input type="checkbox"/> Status Letter  <input type="checkbox"/> Other Enclosure(s) (please identify below):
<b>Remarks</b>  The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.		
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Date	November 16, 2006	Reg. No. 38,581

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**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

**In re Application of:**

Pai-Hung Pan

**Serial No.:** 09/944,506

**Filed:** August 30, 2001

**For:** SHALLOW TRENCH ISOLATION  
STRUCTURE WITHOUT CORNER  
EXPOSURE (as amended)

**Confirmation No.:** 4348

**Examiner:** G. Fourson III

**Group Art Unit:** 2823

**Attorney Docket No.:** 2269-2919.5US

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**APPEAL BRIEF**

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Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R.

§ 41.37(c)(1). The fee required by 37 C.F.R. § 41.20(b)(2) has already been paid.

(1) REAL PARTY IN INTEREST

U.S. Application Serial No. 09/944,506 (hereinafter “the ‘506 Application”), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter “the Office”) at Reel No. 008618, Frame No. 0703. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellants nor the undersigned attorney are aware of any action pending before the Board of Patent Appeals and Interferences (hereinafter “the Board”) that would affect or influence the Board’s decision in the above-referenced appeal.

(3) STATUS OF CLAIMS

The above-referenced application was filed with twenty-four (24) claims.

Claims 8 and 15-17 have been canceled without prejudice or disclaimer.

Accordingly, claims 1-7, 9-14, and 18-24 remain pending and under consideration in the above-referenced application.

Claims 1-6, 13, 14, and 18-24 are subject to final rejections, which are to be reviewed in the above-referenced appeal.

Claims 7 and 9-12 have been allowed.

(4) STATUS OF AMENDMENTS

The '506 Application was filed on September 16, 2003, with twenty-four (24) claims.

A first action on the merits of claim 1-24 was mailed on October 7, 2003. All of the claims were rejected in that Office Action. An Amendment was filed on January 12, 2004, in response to the first Office Action. The Amendment included formal revisions to the claims, as well as explanations as to the patentability of the claims over the numerous objections and rejections that had been presented in the first Office Action.

On April 22, 2004, a second, Final Office Action was mailed. While some of the prior grounds for rejecting the claims were withdrawn, the majority with maintained. Appellants responded by filing an Amendment Under 37 C.F.R. § 1.116 on June 25, 2004, in which the title of the above-referenced application was revised.

Evidently, the Examiner was somewhat convinced by the further reasoning as to the patentability of the claims provided in the Amendment Under 37 C.F.R. § 1.116. The finality of the April 22, 2004, Office Action was withdrawn, and a third, non-final action was issued on July 21, 2004. In the third Office Action, claims 7 and 9-12 were allowed, and claims 5, 14, 20, and 22 were apparently drawn to allowable subject matter. In addition, some of the prior grounds of rejection were maintained and a new ground of rejection was presented. In response to the third action, another Amendment was filed on October 25, 2004. Independent claims 1 and 18 were revised and claims 15-17 were canceled without prejudice or disclaimer. In addition, remarks were provided to show the allowability of the claims that were still rejected.

A fourth, Final Office Action followed on January 11, 2005. That Final Office Action indicated that claims 7 and 9-12 were allowable, but that claims 1-6, 8, 13, and 18-24 were not. In an Amendment Under 37 C.F.R. § 1.116 dated March 11, 2005, Appellants made another attempt to convince the Examiner that the rejected claims are indeed patentable. In addition, claim 8 was canceled, reducing the number of issues that remained for appeal.

The Examiner maintained his rejections in an Advisory Action dated March 29, 2005, and refused to cancel claim 8.

A Notice of Appeal was mailed to the Office on April 7, 2005, and was followed by an Appeal Brief mailed on June 7, 2005.

In an Office Action, mailed on September 6, 2005, the Examiner withdrew the finality of the Final Office Action mailed on January 11, 2005 citing new grounds of rejection. Claim 8 was rejected under obvious type double patenting and claims 1-4, 6, 13, 18, 19, 21, 23, and 24 were rejected under 102(b) as being anticipated by either one of Morita or Mandelman et al. Claim 22 was objected to for containing an informality, claims 7 and 9-12 were allowed, and claims 5, 14, 20, and 22 were apparently drawn to allowable subject matter. Additionally, a rejection under 35 U.S.C. 112, paragraph 1, was withdrawn.

A response to the Office Action, mailed on September 6, 2005, was filed on October 28, 2005 in which Appellants made a final attempt to convince the Examiner that the rejected claims are indeed patentable. A Final Office Action was mailed on December 28, 2005 upholding the objections and the double patenting and 35 U.S.C. § 102(b) rejections.

A response to the Final Office Action was filed on January 27, 2006. The Office Action response included an amendment to claim 22. No further claim amendments have since been presented in the '506 Application.

A Final Office Action was mailed on April 28, 2006 in which the objection to claim 22 was withdrawn, claim 8 was canceled and the 35 U.S.C. § 102(b) rejections were upheld. A response to the Final Office Action was submitted on June 28, 2006.

The Examiner maintained his final rejections in an Advisory Action dated August 1, 2006.

Accordingly, a Notice of Appeal was filed on August 17, 2006, and is followed within two months by this APPEAL BRIEF, which is being submitted by October 17, 2006.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1 of the '506 Application is directed to a precursor to a semiconductor device structure. *See, e.g.*, Fig. 8; paragraphs [0013] and [0021]. That precursor includes a semiconductor device layered structure with at least one trench formed therein. *See, e.g., id.* (including, *e.g.*, reference character 102). A buffer film layer is located over at least a portion of a semiconductor substrate of the semiconductor device layered structure. *See, e.g., id.* (including, *e.g.*, reference character 106). At least one shallow trench isolation (STI) structure is positioned at least partially within the trench. *See, e.g., id.* (including, *e.g.*, reference character 122) The at least one STI structure includes a substantially flat surface and an integral ledge. *See, e.g., id.* The integral ledge extends laterally outward and contacts only an areas of an active surface of the semiconductor substrate that is located adjacent to the at least one trench.

*See, e.g., id.* There is no discernable boundary between the integral ledge and a remainder of the at least one STI structure. *See, e.g.,* Fig. 10; paragraphs [0013] and [0020].

Independent claim 7 is directed to an intermediate semiconductor device structure that includes a semiconductor substrate, a buffer film layer over at least portions of an active surface of the substrate, and at least one densified trench isolation structure. *See, e.g.,* Fig. 8, reference characters 102, 106, 122; paragraphs [0013] and [0020].

Independent claim 13 recites an intermediate semiconductor device structure that includes a semiconductor substrate with at least one trench formed therein and at least one trench isolation structure. *See, e.g.,* Fig. 10, reference characters 102, 126; paragraphs [0013] and [0021]. The at least one trench isolation structure includes a portion that extends laterally over and contacts only a portion of the active surface of the substrate located adjacent to a corner formed between the active surface and a wall of the trench. *See, e.g.,* Fig. 10, reference characters 130, 128; paragraphs [0013] and [0021]. This configuration electrically isolates the at least one trench corner. *See, e.g.,* paragraph [0021].

Independent claim 18 is drawn to a precursor to a semiconductor device structure. The precursor includes a semiconductor substrate and at least one trench formed in the semiconductor substrate. *See, e.g.,* Fig. 8; paragraphs [0013] and [0021]. In addition, the precursor includes a buffer film layer over an active surface of the semiconductor substrate. *See, e.g., id.* (including, *e.g.,* reference characters 102, 106). At least one STI structure is located at least partially within the at least one trench, and is exposed through the buffer film layer. *See, e.g., id.* (including, *e.g.,* reference characters 106, 122). The at least one STI structure includes at least one integral ledge that extends laterally outward from the trench to contact an area of the active surface of the

substrate located adjacent to the trench. *See, e.g., id.* There is no discernable boundary between the ledge and the remainder of the STI structure. *See, e.g.,* Fig. 8; paragraphs [0013] and [0020].

(6) GROUND OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 102(b) rejections of claims 1-4, 6, 13, 18, 19, 21, 23, and 24 for being directed to subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 5,506,168 to Morita et al. (hereinafter “Morita”); and

(B) The rejections of claims 1-4, 6, 13, 18, 19, 21, 23, and 24 under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by the subject matter described in U.S. Patent 5,521,422 to Mandelman et al. (hereinafter “Mandelman”).

(7) ARGUMENT

(A) APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).



(B) ART RELIED UPON

*Morita*

Morita discloses several embodiments of STI structures, most of which include a central region of silicon nitrogen film 37 that fills a trench 2. The only embodiment of an STI structure that includes an integral laterally extending ledge is shown in FIG. 72. More specifically, FIG. 72 of Morita shows an intermediate semiconductor device structure that includes a semiconductor substrate 1 with at least one trench 2 formed therein, silicon oxide films 11 and 36 lining the active surface of the semiconductor substrate 1 and the surfaces of the trench 2, respectively, and silicon nitrogen 37 filling the remainder of the trench 2. *See also*, col. 13, lines 19-26. The silicon oxide film 11 prevents the silicon nitrogen 37 from contacting any portion of the semiconductor substrate 1; the silicon nitrogen 37 instead contacts the silicon oxide film 11 that lines the trench 2 and regions of the active surface of the semiconductor substrate 1 that are adjacent to the trench 2. *See id.*

*Mandelman*

Mandelman describes (at col. 5, lines 3-23) and illustrates (in FIG. 4c) a precursor to a semiconductor device structure that includes a semiconductor substrate 10 with trenches 16 formed therein. The trenches 16 of the semiconductor substrate 10 are lined with a thermal oxide 34, as are areas of the active surface of the semiconductor substrate 10 that are located adjacent to the trenches 16. FIG. 4c; col. 5, lines 3-23. STI structures 18 fill the remaining space within the trenches, and include corner dielectrics 22c that extend laterally over regions of the active surface of the semiconductor substrate 10 that are located adjacent to the trenches 16. *Id.*

The thermal oxide 34 prevents the STI structures 18a and their corner dielectrics 22c from contacting any portion of the semiconductor substrate 10; the STI structures 18a and their corner dielectrics 22c instead contact the thermal oxide 34 that lines the trenches 16 and regions of the active surface of the semiconductor substrate 10 that are adjacent to the trenches 16. *Id.*

(C) ANALYSIS

(1) MORITA

It is respectfully submitted that the description of Morita does not anticipate each and every element of independent claim 1, independent claim 13, or independent claim 18.

Independent claim 1 recites a structure that includes at least one shallow trench isolation structure with a substantially flat surface and an integral ledge that contacts an area of the active surface of a semiconductor substrate of the structure located adjacent to a trench within which the shallow trench isolation structure is at least partially located. There is no discernable boundary between the integral ledge and a remainder of the shallow trench isolation structure.

Independent claim 13 is drawn to an intermediate semiconductor device structure that includes a semiconductor substrate with at least one trench formed therein, and a trench isolation structure within the at least one trench. The trench isolation structure also extends laterally over at least one trench corner and contacts a portion of the active surface of the semiconductor substrate adjacent to a trench corner.

Independent claim 18 is directed to a precursor to a semiconductor device structure. The precursor of independent claim 18 includes a semiconductor substrate, at least one trench formed in the semiconductor substrate, and a buffer film layer over an active surface of the

semiconductor substrate. In addition, the at least one shallow trench isolation structure includes at least one integral ledge that extends laterally outward from the at least one trench so as to contact an area of the active surface adjacent the at least one trench.

The silicon dioxide film 11 and the silicon nitride film 37 described in Morita are fabricated separately from one another and from different materials. As such, the silicon dioxide film 11 is not part of the trench isolation structure 3(37), and, therefore trench isolation structure 3(37) does not contact a surface of the substrate 1. Rather, the trench isolation structure 3(37) contacts the discernably distinct silicon dioxide film 11.

Moreover, assuming, for the sake of argument, that the silicon dioxide film 11 could be considered to be part of a shallow trench isolation structure 3(37), thus allowing for the isolation structure to contact substrate 1, the silicon dioxide film 11 of Morita and, thus, the shallow trench isolation structure 3(37), would also have to be considered to contact more remote portions of the active surface of the substrate than those located laterally adjacent to edges of the trench. This is in contradiction with the requirement of each of independent claims 1, 13 and 18 that an STI structure only contact portions of the active surface that are located “adjacent the at least one trench.”

Additionally, independent claims 1 and 18, by their plain language, require at least one shallow trench isolation structure with no discernable boundary between an integral ledge and a remainder of the at least one shallow trench isolation structure. Because silicon dioxide film 11 and silicon nitride insulation film 37 described in Morita are fabricated separately from one another and made from different materials, there is a discernable boundary between the two

materials, and, therefore, a discernable boundary between exists between the ledge and a remainder of the trench isolation structure.

For these reasons, it is respectfully submitted that the description of Morita does not anticipate each and every element of independent claim 1, independent claim 13, or independent claim 18. As such, each of independent claims 1, 13, and 18 is directed to subject matter that, under 35 U.S.C. § 102(b) is allowable over the disclosure of Morita.

Claims 2-4 and 6 are each allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

Each of claims 19, 21, 23, and 24 is allowable, among other reasons, for depending directly or indirectly from independent claim 18, which is allowable.

(2) MANDELMAN

It is respectfully submitted that the description of Mandelman does not anticipate each and every element of any of independent claim 1, independent claim 13, or independent claim 18.

The STI structure 18 and thermal oxide layer 34 described in Mandelman are fabricated separately from one another and from different materials. Therefore, the thermal oxide layer 34 is not part of the STI structure 18, and, therefore, the corner dielectric 22c of STI structure 18 does not contact the active surface of the substrate 10. Rather, the corner dielectric 22c of STI structure 18 contacts the discernably distinct thermal oxide layer 34. Therefore, Mandelman does not anticipate a shallow trench isolation structure with an integral ledge that contacts an area of an active surface of a semiconductor substrate adjacent to at least one trench, as required by independent claims 1, 13, and 18.

Additionally, the manner in which the oxide layer 34 and STI structure 18 of Mandelman are formed results in a discernable boundary between these elements, contrary to the requirement of independent claims 1 and 18 that there be no discernable boundary between a ledge of a shallow trench isolation structure and the remainder of the shallow trench isolation structure.

As such, Mandelman does not anticipate each and every element of any of independent claim 1, independent claim 13, or independent claim 18, as would be required to maintain the 35 U.S.C. § 102(b) rejections of these claims.

Claims 2-4 and 6 are each allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

Each of claims 19, 21, 23, and 24 is allowable, among other reasons, for depending directly or indirectly from independent claim 18, which is allowable.

In view of the foregoing, reversal of the 35 U.S.C. § 102(b) rejections of independent claims 1, 13, 18 and the claims that depend therefrom is respectfully solicited.

(8) CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

(9) EVIDENCE APPENDIX

There is no EVIDENCE APPENDIX to this APPEAL BRIEF.

(10) RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application.

Therefore, this Appeal Brief is not accompanied by a RELATED PROCEEDINGS APPENDIX.

(11) CONCLUSION

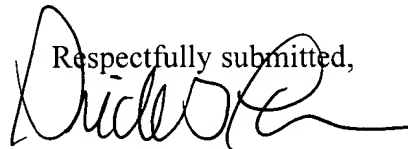
It is respectfully submitted that:

(A) Claims 1-4, 6, 13, 18, 19, 21, 23, and 24 are allowable under 35 U.S.C. § 102(b) for reciting subject matter which is patentable over that described in Mandelman; and

(B) Claims 1-4, 6, 13, 18, 19, 21, 23, and 24 are also allowable under 35 U.S.C. § 102(b) for being directed to subject matter that is novel over the subject matter described in Morita.

Accordingly, it is respectfully requested that the rejections of claims 1-6, 13, 14, and 18-24 be reversed and that each of these claims be allowed.

Respectfully submitted,



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Date: November 16, 2006

JPN/eg

Document in ProLaw



Serial No. 09/944,506

## CLAIMS APPENDIX

1. (Previously presented) A precursor to a semiconductor device structure, comprising:  
a semiconductor device layered structure comprising a semiconductor substrate;  
a buffer film layer located over at least a portion of the semiconductor substrate;  
at least one trench formed in the semiconductor device layered structure; and  
at least one shallow trench isolation structure positioned at least partially within the at least one trench and including:  
a substantially flat surface; and  
an integral ledge which extends laterally outward from the at least one trench, with no discernable boundary between the integral ledge and a remainder of the at least one shallow trench isolation structure, so as to contact only an area of an active surface of the semiconductor substrate adjacent the at least one trench.
2. (Previously presented) The precursor of claim 1, wherein the buffer film layer comprises substantially oxidation resistant material.
3. (Previously presented) The precursor of claim 2, wherein the substantially oxidation resistant material is selectively etchable.
4. (Previously presented) The precursor of claim 1, wherein a lateral edge of the integral ledge contacts the buffer film layer.

5. (Previously presented) The precursor of claim 1, wherein the at least one shallow trench isolation structure comprises densified material.

6. (Previously presented) The precursor of claim 1, wherein the buffer film layer comprises silicon nitride.

7. (Previously presented) An intermediate semiconductor device structure, comprising:  
a semiconductor substrate including at least one trench formed therein and at least one trench corner located at a juncture between the at least one trench and an active surface of the semiconductor substrate; and  
a buffer film layer over at least portions of the active surface; and  
at least one densified trench isolation structure including a substantially flat surface exposed through the buffer film layer, the at least one trench corner being covered by the at least one densified trench isolation structure.

8. (Canceled)

9. (Previously presented) The intermediate semiconductor device structure of claim 7, further comprising:  
a layer comprising silicon oxide disposed within the at least one trench and between the semiconductor substrate and the buffer film layer.



10. (Previously presented) The intermediate semiconductor device structure of claim 9, wherein the layer comprises densified silicon dioxide.

11. (Previously presented) The intermediate semiconductor device structure of claim 7, wherein the at least one densified trench isolation structure comprises densified material.

12. (Previously presented) The intermediate semiconductor device structure of claim 7, wherein the buffer film layer comprises silicon nitride.

13. (Previously presented) An intermediate semiconductor device structure, comprising:  
a semiconductor substrate including at least one trench formed therein and at least one trench corner located at a juncture between the at least one trench and an active surface of the semiconductor substrate; and  
at least one trench isolation structure including a substantially flat surface, the at least one trench isolation structure extending laterally over and contacting only a portion of the active surface adjacent the at least one trench corner so as to electrically isolate the at least one trench corner.

14. (Previously presented) The intermediate semiconductor device structure of claim 13, wherein the at least one trench isolation structure comprises densified silicon dioxide.

15-17. (Canceled)

18. (Previously presented) A precursor to a semiconductor device structure, comprising:  
a semiconductor substrate;  
at least one trench formed in the semiconductor substrate;  
a buffer film layer over an active surface of the semiconductor substrate;  
and at least one shallow trench isolation structure at least partially within the at least one trench  
and exposed through the buffer film layer, the at least one shallow trench isolation  
structure including at least one integral ledge extending laterally outward from the at least  
one trench, with no discernable boundary between the at least one integral ledge and a  
remainder of the at least one shallow trench isolation structure, so as to contact an area of  
the active surface adjacent the at least one trench.

19. (Previously presented) The precursor of claim 18, wherein the at least one shallow  
trench isolation structure includes a substantially planar surface.

20. (Previously presented) The precursor of claim 18, wherein the at least one shallow  
trench isolation structure comprises densified silicon oxide.

21. (Previously presented) The precursor of claim 18, wherein the buffer film layer  
comprises silicon nitride.

22. (Previously presented) The precursor of claim 18, wherein the at least one shallow trench isolation structure comprises densified material.

23. (Previously presented) The precursor of claim 18, wherein the buffer film layer comprises substantially oxidation resistant material.

24. (Previously presented) The precursor of claim 23, wherein the substantially oxidation resistant material is selectively etchable.



**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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Pai-Hung Pan

**Serial No.:** 09/944,506

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**COMMUNICATION ACCOMPANYING APPEAL BRIEF**

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P.O. Box 1450  
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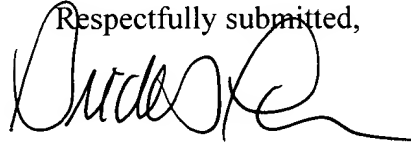
This communication is accompanied by an Appeal Brief that has been revised pursuant to the Notification of Non-Compliant Appeal Brief that was mailed on October 30, 2006.

The Notification indicated that the previously submitted Appeal Brief was non-compliant for lacking a proper SUMMARY OF CLAIMED INVENTION section. The specific reasoning behind the objections to the Appeal Brief is unclear from the Notification. Upon review of the pertinent Rules, it is respectfully submitted that the originally filed Appeal Brief was in full compliance with the Rules.

In any event, the SUMMARY OF CLAIMED INVENTION section of the Appeal Brief has been revised to more clearly identify the subject matter associated with each independent claim. It is noted that the as-filed specification of the above-referenced application lacks columns and line numbers and, instead, includes paragraph numbers, as has now been common practice before the U.S. Patent & Trademark Office for several years. Accordingly, for the sake of clarity, reference to the specification is made by way of the paragraph numbers that have been set forth in the specification, rather than to the specific column and line numbers. In addition, reference to non-limiting examples of the claimed subject matter, as set forth in the drawings of the above-referenced application, have also been included in the SUMMARY OF CLAIMED INVENTION.

If there are any additional issues that need to be resolved before the Appeal Brief may be considered, an explanation as to the legal basis for such issues and the identification of specific parts of the Appeal Brief that need to be revised would be appreciated.

Respectfully submitted,



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